REMARKS

Claims 1-23 are pending in the application. Claims 1-3, 8, 10, 11, 14-18, 22, and 23 have been amended.

Claims 1-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Number 5,526,024 to Gaglianello et al. ("Gaglianello").

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaglianello in view of U.S. Patent Number 5,917,959 to Kagawa et al. ("Kagawa").

Applicants respectfully traverse the rejections in view of the amendments and the following remarks.

Claims 1-7

Claim 1 has been amended to recite a line buffer. Gaglianello certainly does not anticipate claim 1, at least because Gaglianello does not teach or suggest "setting an indicator in a line buffer" as recited in claim 1.

The rejection cites column 1 lines 50-67 and column 2 lines 2-11 of Gaglianello. However, the cited portion of Gaglianello is clearly limited to partitioning a frame buffer rather than a line buffer.

Gaglianello clearly himself explains the difference between a frame buffer and a line buffer, stating that:

> Frame buffer 18 outputs the data to display screen 20. Although not explicitly shown in the drawing, a line buffer is illustratively interposed between the frame buffer and the display screen to store successively lines of data as they are presented for display on the display screen.

(See column 2, lines 58-62 of Gaglianello).

Additionally, Gaglianello teaches that "In an illustrative embodiment of the invention, undesirable artifacts are prevented by partitioning the frame buffer of the workstation display into two or more segments. Each segment includes one or more rows of the frame buffer, each row storing a line of video data." (See column 1, lines 61-65 of Gaglianello).

That is, Gaglianello teaches that each segment stores at least one full line of video data. Therefore, the frame buffer must include at least two full lines of data (at least one full line for each of the two segments). Therefore, the frame buffer of Gaglianello is limited to being more than one line and is not a line buffer. In practice, a frame of video data typically includes many lines of video data rather than two.

Further, there is no motivation to modify Gaglianello to use a line buffer with an indicator rather than or in addition to "partitioning the frame buffer of the workstation display into two or more segments." (See column 1, 62-63 of Gaglianello). The motivation provide an indicator in a line buffer comes from Applicants' specification alone, which states that, e.g., "higher memory bandwidth is needed to ensure the pixel processing is completed in sufficient time to display the next overlay scan line." (See the specification, page 2, lines 5-7).

Claims 2-7 depend from claim 1, and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claim 8

Applicants have amended claim 8 to recite a line buffer. Gaglianello certainly does not anticipate claim 8, at least because Gaglianello does not teach or suggest "loading data for the next video line into the line buffer when the video data for the current video line is located at a predetermined position," as recited in claim 8 (see the discussion of claim 1 above).

Claims 9-13 depend from claim 8, are therefore patentable over Gaglianello for at least the same reasons as stated above with respect to claim 8.

Claims 14-17

Applicants have amended claim 14 to recite a line buffer. Gaglianello certainly does not anticipate claim 14, at least because Gaglianello does not teach or suggest "an indicator positioned at a predetermined memory location in the line buffer" as recited in claim 14 (see the discussion of claim 1 above).

Since claims 15-17 depend from claim 14, they are patentable over Gaglianello for at least the same reasons stated above with respect to claim 14.

Claims 18-21

Claim 18 has been amended to recite a line buffer. Gaglianello certain does not anticipate claim 18, at least because Gaglianello does not teach or suggest "a line buffer which receives the video data from the memory, wherein said line buffer includes an indicator positioned at a predetermined memory location in the line buffer," as recited in claim 18 (see the discussion of claim 1, above).

Claims 19-21 depend from claim 18, and are therefore patentable for at least the same reasons as stated above with respect to claim 18.

Claim 21 was rejected under 35 U.S.C. 103 as being unpatentable over Gaglianello in view of Kagawa. However,

Kagawa does not remedy the deficiencies of Gaglianello as described above with respect to claim 18. Therefore, claim 21 is patentable over Gaglianello and Kagawa, alone or in combination.

Claims 22 and 23

Claim 22 has been amended to recite a line buffer. Gaglianello certainly does not anticipate claim 22, at least because Gaglianello does not teach or suggest "set an indicator in a line buffer," as recited in claim 22.

Claim 23 depends from claim 22 and is therefore patentable for at least the same reason as stated above with respect to claim 22.

Attached is a marked-up version of the changes being made by the current amendment.

CONCLUSION

For at least the above reasons, Applicants believe that claims 1-23 are in condition for allowance, and ask that all claims be allowed. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (858) 678-5070.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7/12/02

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Version with markings to show changes made

In the claims:

Claims 1-3, 8, 10, 11, 14-18, 22, and 23 have been amended as follows:

1. (Amended) A method comprising:

setting an indicator in a line buffer;

reading pixel data for a current video line from the line buffer;

determining when the pixel data reaches the indicator; and

loading data for the next video line into the line buffer.

2. (Amended) The method of Claim 1, further comprising setting the indicator at approximately a middle of the line buffer.

3. (Amended) The method of Claim 1, further comprising loading data for the next video line to replace data for the current video line in the line buffer.

8. (Amended) A method of processing video overlay data comprising:

reading video data for a current video line from a line buffer;

detecting the position in the line buffer the video data is located;

loading data for the next video line into the line buffer when the video data for the current video line is located at a predetermined position.

10. (Amended) The method of Claim 8, further comprising setting the predetermined position at approximately a midpoint of the line buffer.

11. (Amended) The method of Claim 8, further comprising loading data for the next video line to replace data for the current video line in the line buffer.

14. (Amended) A overlay display processor comprising:

a line buffer having a plurality of memory locations, the line buffer adapted to provide data to a display; and

an indicator positioned at a predetermined memory location in the line buffer, wherein the line buffer begins to read data for a next video data line when the line buffer provides data from the indicator memory location.

15. (Amended) The computer of Claim 14, further comprising graphic memory which provides the video pixel data to the line buffer.

16. (Amended) The computer of Claim 14, wherein the line buffer provides data to the display for a current video line.

17. (Amended) The computer of Claim 14, wherein the indicator is located at a position at approximately a midpoint of the line buffer.

18. (Amended) A overlay display system comprising:

video memory which stores video data;

an overlay processing engine comprising:

a line buffer which receives the video data from the memory, wherein said line buffer includes an indicator positioned at a predetermined memory location in the line buffer;

video processing circuitry for preparing the video data in the line buffer to be displayed; and

a display which receives the processed data from the overlay processing engine, wherein the line buffer begins to read data for a next video data line when the line buffer provides a predetermined amount of data to the display for a current video data line.

22. (Amended) A program storage device readable by a machine comprising instructions that cause the machine to:

set an indicator in a line buffer;

read pixel data for a current video line from the line buffer;

determine when the pixel data reaches the indicator; and

load data for the next video line into the line buffer.

23. (Amended) The program storage device of Claim 22, wherein the instructions further cause the machine to set the indicator at approximately a middle of the line buffer.